Request for Information (RFI)

Low-Dimensional Materials for Power-Performance-Area (PPA) Optimization in Logic Applications Beyond CFET

Issued: May 2025

Deadline for submissions: June 2, 2025

Submission portal: https://natcast.secure-platform.com/rnd

Overview: Natcast, the operator of the National Semiconductor Technology Center (NSTC), is seeking public input on the focus and prioritization of a potential research program on the use of low-dimensional (low-D) materials for Power-Performance-Area (PPA) optimization in novel devices to support AI computing requirements that will bridge the lab-to-fab gap for these materials.

Low-dimensional materials, including 1D materials like carbon nanotubes (CNTs), 2D materials such as graphene and transition metal dichalcogenides (TMDs), and others offer unique electrical properties that could significantly enhance device performance. These materials have the potential to enable further scaling and provide superior performance characteristics compared to traditional silicon-based technologies.

Despite their promise, integrating low-D materials into high volume manufacturing presents significant challenges such as developing reliable synthesis methods, ensuring material uniformity, and achieving compatibility with existing and future fabrication processes.

The primary objective of this RFI is to gather insights and recommendations from a broad range of stakeholders to help shape a concerted effort to transition from proof-of-concept demonstrations in the lab to reliable and scalable manufacturing solutions.

Who should respond: This Request for Information (RFI) seeks input from a broad range of organizations that may benefit from such a research program: foundries, integrated device manufacturers (IDMs), materials suppliers, equipment vendors, academia, startup companies, small businesses, technology incubators, government labs, federally funded research and development centers (FFRDCs), university applied research centers (UARCs), the defense industrial base, and other commercial semiconductor companies.

This announcement is not a request for proposal submission. Any costs incurred by interested parties in response to this announcement will not be reimbursed. Respondents acknowledge that by participating in this RFI, they grant Natcast permission to use the contact details provided in the response for direct communication concerning this RFI and any subsequent collaborations.

To submit a response to this RFI:

- Responses should be provided in PDF format, not to exceed 5 pages. Any references, tables of acronyms, or title pages would not count towards the page count. Partial responses are acceptable. Not all questions need to be addressed.
- Please clearly mark confidential business information or other nonpublic information in your response. Be advised that Natcast may share a summary of aggregated response data with the Department of Commerce and/or other third parties, including potential release to the public. This summary will not include respondents' individual submissions, or any confidential or identifying information. By submitting your response, you consent that information from your response may be aggregated as part of that summary.
- Responses must be submitted no later than 5PM ET on June 2, 2025.

To submit your response, please complete the web form for the R&D Request for Information at https://natcast.secure-platform.com/rnd and upload your document. Submit any questions to research@natcast.org.

RFI Questions and Discussion Topics

1. Background
    a. Submissions should include the following information:
        i. Organization name
        ii. Size of organization in either revenue or employees, as appropriate
        iii. Title of primary point of contact
        iv. Email of the primary point of contact
    b. Briefly describe your current organization in a paragraph. Feel free to include a web link for further information. Do not include large corporate overview presentations.
    c. Have you participated in or do you plan to participate in other CHIPS Act programs?
    d. Describe your prior and current interests and work in low-D materials for advanced logic CMOS applications and provide examples including, but not limited to, publications, presentations, patents, etc.
2. What are the most critical areas (i.e. channel, middle of line, local interconnect, etc.) within CMOS transistor technology and other device components where low-D materials can provide the greatest benefits? What are the best metrics for evaluating or quantifying the benefits?
3. Which low-D materials should be prioritized based on their potential for PPA optimization and their readiness for integration into semiconductor manufacturing processes?

4. Based on your experience, what is the time horizon for integrating low-D materials into a competitive CMOS device (with demonstrated comparable/superior electrical performance to Si) which enables scaling beyond CFET? Please be specific about which material and whether it is 1D or 2D.
5. What are the key opportunities for accelerating this timeline via NSTC R&D funding? Note that NSTC R&D funding can extend to shared use infrastructure, with examples such as the EUV Accelerator, the Design Enablement Gateway, or the Test Vehicle Innovation Pipeline.
6. What are the biggest challenges for low-D materials synthesis. Please highlight specific challenges for specific materials and whether it is 1D or 2D? Mention any other relevant challenges, such as benchmarking, measurement, etc.
7. What are the most promising methods for synthesizing and integrating low-D materials at wafer scale (200 mm to 300 mm)?
8. What are the biggest challenges for low-D material CMOS fabrication at the laboratory or coupon scale? What are the biggest challenges at a 200- or 300-mm scale? In high volume manufacturing? How do these relate? Examples of challenges include:
    a. Transferring processes from coupons to 200- or 300-mm wafers
    b. Material physical characterization in either the laboratory or inline
    c. Thermal processing limitations
    d. Surfaces and interfaces optimization
    a. Integration in the CMOS flow: high-k/metal gate, source-drain, contacts, auxiliary materials (e.g. spacers, liners, dummy fills)
    b. Patterning to prove device characteristics at sub-2nm CMOS node
    c. Device characterization including statistical variation and reliability
9. Beyond the technical challenges, what are the logistical, institutional, and organizational challenges involved in transitioning low-D materials from laboratory research to commercial production?
10. For an organization such as yours, what type of partnerships and research funding would be required to form a holistic research effort on low-D CMOS devices directly translating to an industrially relevant prototype?
11. Please suggest anything else that we should consider when formulating this research program.