U.S. NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER

Introducing NSTC Membership

October 18, 2024

Disclaimer

- Statements and responses to questions about advanced microelectronics research and development programs in this presentation:
  - Are informational, pre-decisional, and preliminary in nature.
  - Do not constitute a commitment and are not binding on NIST or the Department of Commerce.
  - Are subject in their entirety to any final action by NIST or the Department of Commerce.
- Nothing in this presentation is intended to contradict or supersede the requirements published in any future policy documents or funding opportunities.

The CHIPS & Science Act

$39B
Incentives

Invest in U.S. production of strategically important semiconductor chips, and assure a sufficient, sustainable, and secure supply of older and current generation chips for national security purposes and for critical manufacturing industries.

$11B
R&D

Strengthen U.S. semiconductor research and development (R&D) leadership to catalyze and capture the next set of critical technologies, applications, and industries.

$2B
DoD

The DoD Microelectronics Commons is a national network that will create direct pathways to commercialization for US microelectronics researchers and designers from “lab to fab.”

Workforce Initiatives

Four CHIPS R&D programs

CHIPS
National Semiconductor Technology Center (NSTC) Program

CHIPS
National Advanced Packaging Manufacturing Program (NAPMP)

CHIPS
Manufacturing USA Program

CHIPS
Metrology Program

Workforce Initiatives

NSTC Vision and Goals

The NSTC will become an essential resource within the semiconductor ecosystem, leveraging its network of scientists and engineers, state-of-the-art facilities, and collaborative programs to deliver large-scale technical achievements and impact.

Semiconductor ecosystem goals = NSTC strategic goals

1. **Extend U.S. semiconductor leadership**
2. **Reduce time and cost to prototype**
3. **Build a robust workforce ecosystem**

Goal 1.

Extend U.S. semiconductor technology leadership

The NSTC will reinforce and extend U.S. technology leadership in semiconductors by identifying and advancing promising research initiatives in foundational semiconductor technologies.

- Focus on the early stage of “lab-to-fab” gap, helping ideas achieve a proof-of-concept or validation point
- Execute research agenda through research awards, in-house and member-driven research

Strategic Objectives

- **Jump start research program**
- **First research agenda**
- **Long-term research programs**
- **Convenings**

Goal 1.

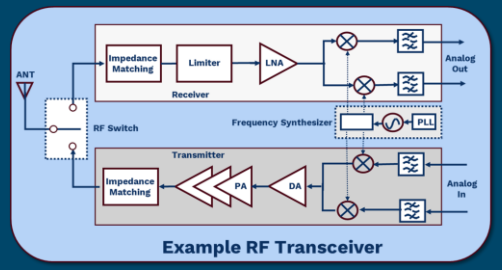
NSTC R&D Jump Start Programs

Stay Tuned for R&D Topic #4

Pending Award(s)

AIDRFIC

- Up to $30M for AI Driven RF Design with 3-4 awardees anticipated



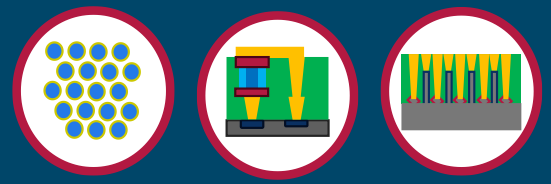
Example RF Transceiver

- Proposal submission is closed
- 75+ unique entities teamed and responded to call for proposals
- Final Selection
- Anticipated Project Start Jan. 2025

Under Solicitation

TVIP

- Up to $55 Million for Test Vehicles Innovation Pipeline with 4-12 awardees anticipated
- Standardized Test Structures and Resource Optimization for Early-Stage R&D for the following focus areas:

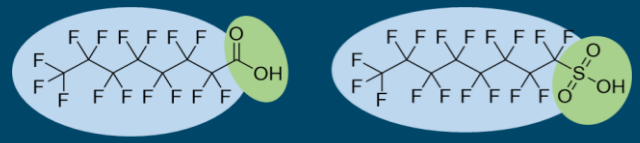

EUV Scale Process | CMOS + X Test Chips | FEOL/MEOL Materials

- Full Proposals Due Oct. 21, 2024
- Target Project Start April 2025

Call Coming Soon

PFAS

- Anticipate releasing a call for proposals for semiconductor PFAS abatement in the coming weeks
- Focus on developing and improving methods to reduce, measure, and abate PFAS emissions in semiconductor manufacturing



PFOA – C_8 | PFOS – C_8

- Foster collaboration and information sharing within the ecosystem to address PFAS use effectively

Launched Early Jump Start Projects this Summer with $100M+ Invested

Goal 2.

Reduce the time and cost to prototype

NSTC will reduce the time and cost to explore, prototype, and validate innovative semiconductor designs and technology.

- Establish a portfolio of physical/ digital assets, services, and capital (e.g., facilities, Design Enablement Gateway, silicon aggregation services, innovation fund)
- Streamline access to tools and facilities, opportunities for experimentation

Strategic Objectives

- **Facilities**
- **Design Enablement Gateway**
- **Silicon aggregation services**
- **Investment fund**

Goal 3.

Build and sustain a semiconductor workforce development ecosystem

NSTC Workforce Center of Excellence (WCoE) will be an anchor institution tasked with coordinating national workforce development efforts to support the semiconductor industry of tomorrow.

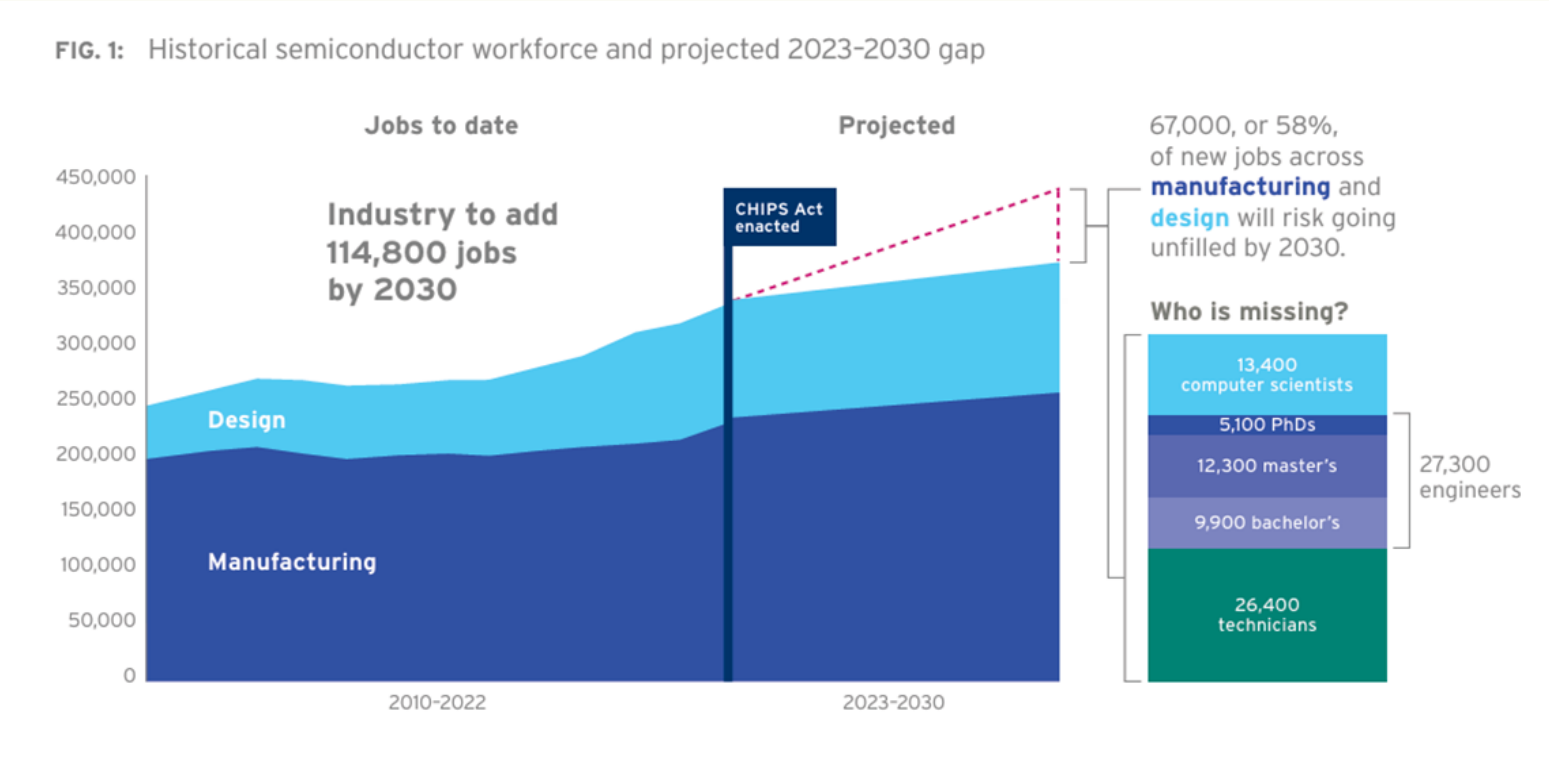
Guiding Principles:

- Increase employer access to talent
- Increase individual's access to opportunity in the industry

Strategic Objectives

- **Partnership, funding, & recognition programs**
- **WCoE digital clearinghouse**
- **Technical assistance program**
- **Data collection and research program**

The next generation of talent



[1] *Semiconductor Industry Association, "Chipping Away: Assessing and Addressing the Labor Market Gap Facing the U.S. Semiconductor Industry", July 2023.*

By 2030, **67,000 jobs risk going unfilled across the U.S. semiconductor industry.** We must work urgently to address:

- **Employer requirements** for forecasted industry roles
- The **lack of awareness** of the industry among individuals
- The **insufficient number** of individuals prepared by U.S.-based programs
- **Losing potential talent to other fields**

Goal 3.

Workforce Center of Excellence program offices

Our Programs

WCoE **Signals**	*WCoE* **Amplifier**	*WCoE* **Connections**
Harness the power of data to **discover best practices, share insights and monitor progress**.	**Scale effective workforce development** practices through funding and recognizing best practices.	**Equip members with the tools** they need to overcome challenges and grow the workforce**.**
Representative activities		
Workforce supply and demand data	Grants and awards	Workshops
Research and publications	Recognition program	Custom workforce services
Digital repository of resources & tools	Partnership opportunities	Webinars and events

Goal 3.

Workforce Partner Alliance Program (WFPA)

The WFPA program is the first of several anticipated workforce program funding opportunities to be offered through the NSTC Workforce Center of Excellence focused on investing in training for careers in the semiconductor industry.

Key Principles

- **Alignment with employer needs**
- **Scaled for meaningful impact**
- **Integrated with regional ecosystems**
- **Supported by industry**

Applications for the Workforce Partner Alliance program were assessed on several factors, including, but not limited to:

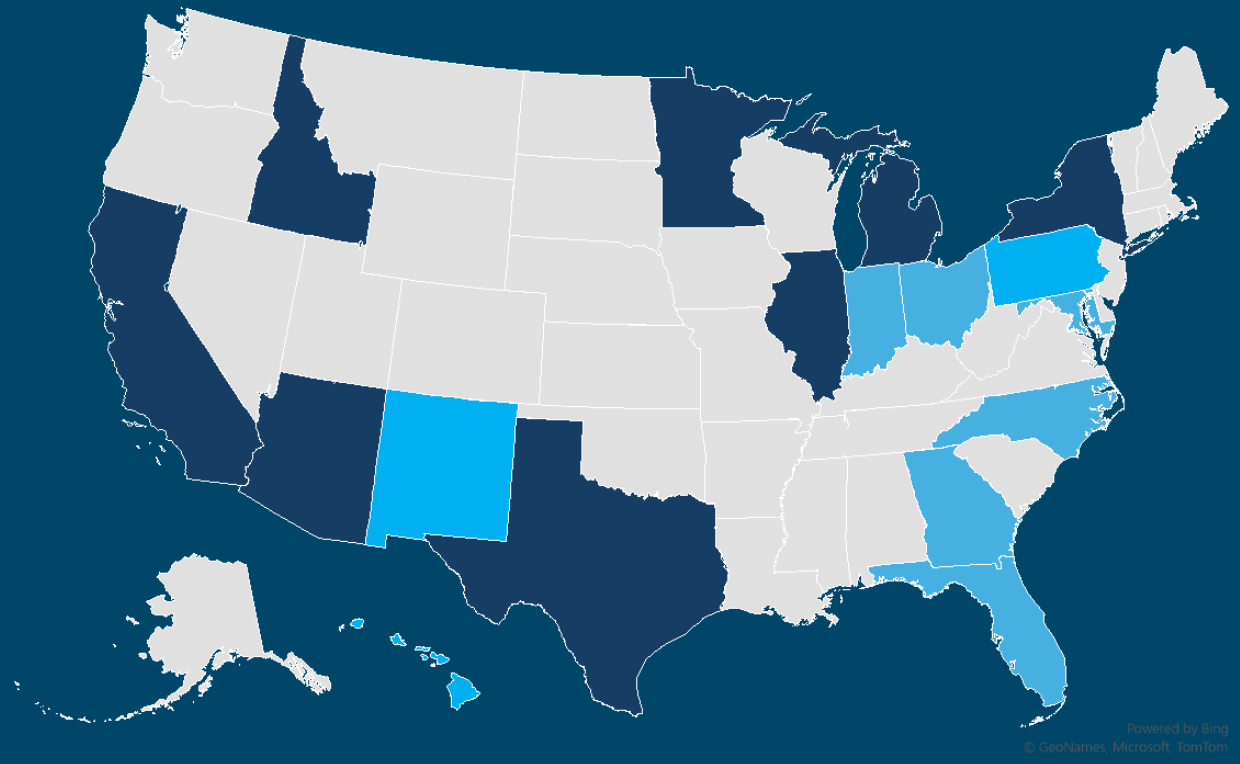
- Likely effectiveness of the planned approach
- Alignment of the program with the needs of semiconductor employers
- Potential economic and quality-of-life impact on program participants
- Scale of impact
- Ability to foster partnerships with local community organizations
- Engagement of underserved communities

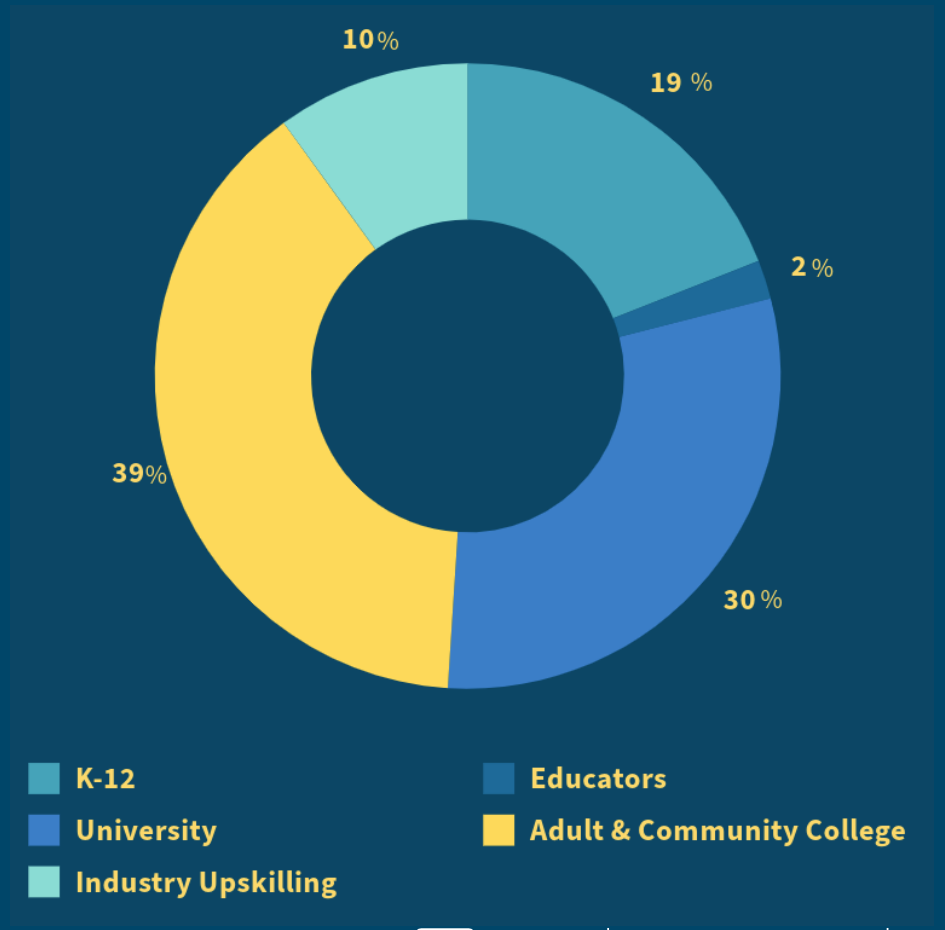
Goal 3.

Workforce Partner Alliance Program (WFPA)

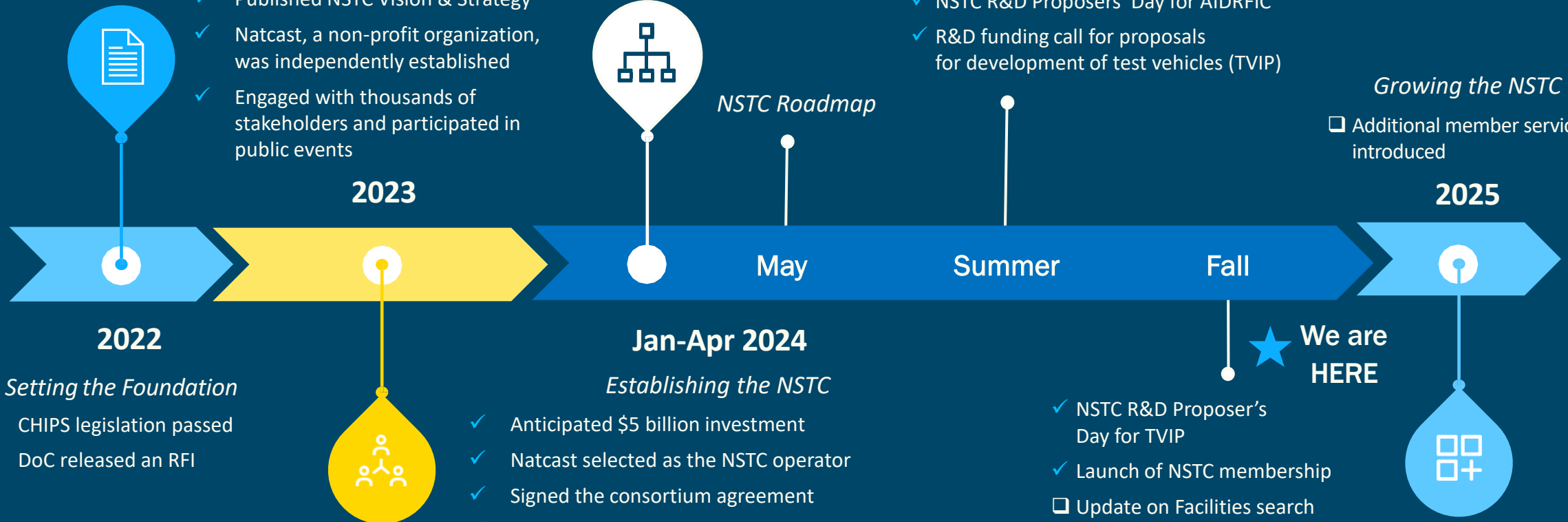
7 anticipated awardees - $11.5M

NSTC WORKFORCE PARTNER





NSTC Roadmap: 4 Year View



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Our members create the technologies that transform the world.

Membership

NSTC Membership – Launched Sept. 30

Design	Academia	Professional Services
Manufacturers	End Customers	Workforce Intermediaries
Investors	Govt. Organizations	Suppliers

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Guiding Principles

Accessible

Valuable

Simple

Connected

Membership categories

Two categories of membership support our diverse ecosystem

Core Members

Entities directly involved in technology development or the design of materials, tools, chips, or systems that use semiconductors

Example groups:

- Companies (large & small)
- Research-focused academic institutions
- Consortia that are legal entities
- National, state, private research labs
- Government agencies focused on semiconductor R&D

Affiliate Members

Entities not directly involved in semiconductor technology development or the design of materials, tools, chips, or systems that use semiconductors

Example groups:

- Investors
- Academic institutions not focused on research
- Workforce stakeholders
- Consortia that are legal entities
- Government agencies not focused on semiconductor R&D
- Professional services

NSTC service offerings

Three pillars: Innovate, Collaborate, Educate

Innovate

Create opportunities that drive technology innovation across semiconductor industry

Collaborate

Encourage and facilitate interaction and collaboration among NSTC membership

Educate

Collect, build, share, and expand educational resources/ capabilities/programs

Member Concierge

Anticipated member benefits

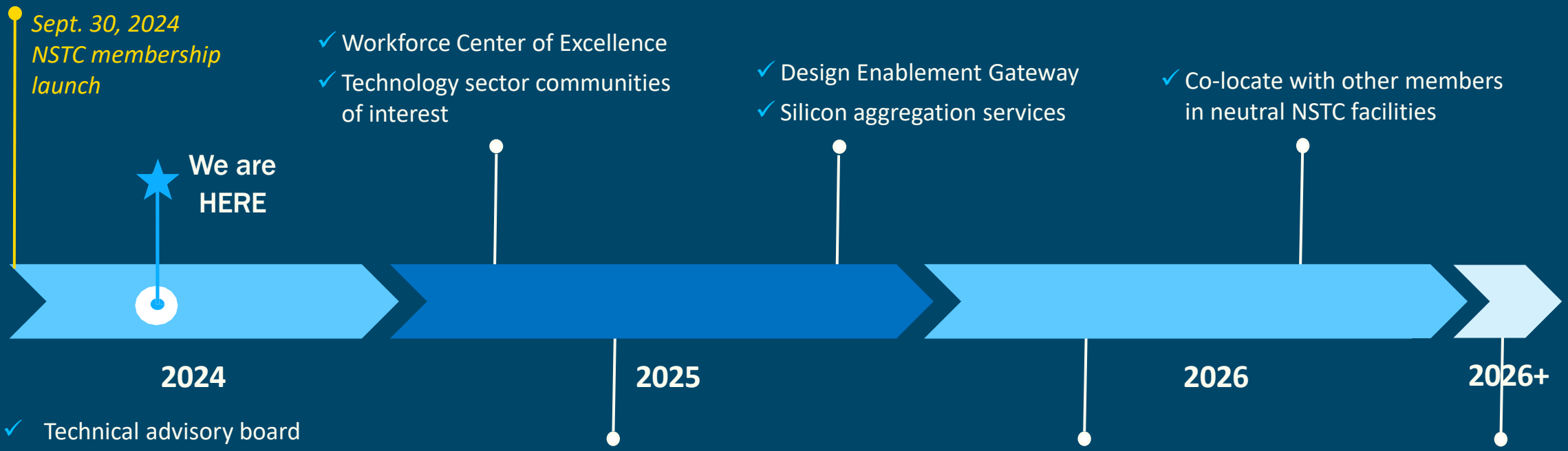
Benefits	Anticipated Availability
Educate	
Access to reports, news, webinars, seminars	Now
Eligibility for workforce funding opportunities	Now
Access to Workforce Center of Excellence resources and programs	2025
Access to workforce program experts	2025
Collaborate	
Access to NSTC Conferences & events to network with other members and learn about the industry	Now
Eligibility for Workforce Advisory Board (WFAB) to guide workforce priorities	Now
Eligibility for Technical Advisory Board (TAB) to guide research agenda	Now
Teaming and co-development to learn from and work with other members	Now
Ability to participate in technology sector communities of interest	2025
Co-location opportunities with other members in neutral NSTC facilities*	2026
Innovate	
Eligibility for research grant awards to fund R&D initiatives	Now
Ability to participate in member-funded research projects*	2025
Design Enablement Gateway to reduce time and cost to design and facilitate collaboration*	2025
Silicon aggregation services to access multi-project wafers and other production needs*	2025
Ability to participate in NSTC-led research projects	2026
Eligible to license NSTC IP assets*	2026
Opportunities to present to partner investment funds to earn additional funding	2026
Facilities providing prototyping and development opportunities*	2026+

Affiliate Membership

Core Membership

** indicates additional fee for access and usage*

Anticipated availability of member benefits



- ✓ Technical advisory board
- ✓ Research grant awards
- ✓ Workforce advisory board
- ✓ Workforce grant awards
- ✓ Workforce program experts
- ✓ Reports, news, webinars, seminars
- ✓ NSTC conferences and events
- ✓ Collaborate with other members

- ✓ Workforce Center of Excellence
- ✓ Technology sector communities of interest

- ✓ Member-funded research
- ✓ More research grant awards
- ✓ More workforce grant awards

- ✓ Design Enablement Gateway
- ✓ Silicon aggregation services

- ✓ Investment fund
- ✓ NSTC-led research
- ✓ License NSTC IP assets
- ✓ More research grant awards
- ✓ More workforce grant awards

- ✓ Co-locate with other members in neutral NSTC facilities

- ✓ Facilities providing prototyping and development opportunities*

NSTC membership value proposition

Benefits for all

- Guide research agenda
- Collaborative R&D
- Access to new technologies & IP
- Cross-ecosystem connections and collaboration
- Workforce Center of Excellence and awards
- Ecosystem insights /trends

Member-specific benefits

- Access to facilities and experts
- New Business Opportunities
- Investment and VC opportunities
- Technical residency & Internships
- Data from facilities, processes and products
- Promotion of research
- Design Enablement Gateway & silicon aggregation services
- Diversify supply chain
- Research awards
- Prototyping and evaluation of new concepts
- Test & validate new materials & equipment in full flow processes
- Coordinate on development of new standards

Member Concierge

Eligibility

✓ **Legal entity**[1]	Individuals and sole proprietors are not eligible for membership in the NSTC.
✓ **U.S. presence**	NSTC Members shall have a meaningful U.S. presence at the time of membership and maintain a U.S. presence.
✓ **Not a FEOC / FCOC**	Foreign Entities of Concern or Foreign Countries of Concern are not eligible for membership.

1. Eligible legal entities include but are not limited to: companies, academic institutions, consortia operators, government agencies focused on semiconductor R&D, investors, workforce intermediaries, and more.

IP guiding principles

1. Flexibility to accommodate different NSTC program objectives

2. Performers will retain ownership of the IP they develop; however, generalizable insights, outcomes and data may be shared with the NSTC members to foster broader innovation

3. Encourage member engagement

4. Account for the technology's maturity level

5. Enhance U.S. economic competitiveness and protect national security concerns

Membership pricing framework

	Base Fees	Access Fees	Usage Fees
Affiliate	✓ Flat fee by member segment	N/A	N/A
Core	✓ Tiered by member segment and size[1]	✓ Tiered by member segment and size[1] ✓ Applicable to some services[2]	✓ Same fee structure across all members ✓ Applicable to some services[2]

Visit natcast.org/NSTCmembership for a detailed base membership fee schedule

1. Depending on the member segment, tiering is based on semiconductor revenues, total revenues, or federal R&D expenditures
2. Facilities, Design Enablement Gateway, silicon aggregation services, NSTC IP

Together, our members innovate for the future.

Join us.

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Let's Get Started:

- Subscribe to our mailing list: natcast.org/newsletter
- Complete NSTC Membership application: natcast.org/NSTCmembership
- Submit Technical Advisory Board (TAB) application
- Identify key leaders to engage
- Participate in workshops and focus groups on technology, IP and workforce

Events

Join us at the NSTC Symposium

October 28-30

Omni Shoreham, Washington, D.C.

The 2024 NSTC Symposium and ME Commons Annual Meeting will feature three days of programming from U.S. microelectronics leaders from industry, academia, and government, including the Department of Defense and the Department of Commerce. Both events offer exclusive insight into the achievements made through the CHIPS and Science Act to date and how the nation is being mobilized to establish collaboration-based infrastructure to revitalize U.S. microelectronics technological advancement, onshoring efforts, and workforce development.

Learn more: natcast.org/news

In collaboration with ME Commons

Day 1: NSTC Symposium

October 28, 2024
8:30 AM - 5:30 PM

Opening Remarks
Featuring The Honorable U.S. Secretary of Commerce Gina Raimondo and Dr. Laurie Locascio, Under Secretary of Commerce for Standards and Technology and Director of the National Institute of Standards and Technology (NIST).

NSTC & Natcast Overview
An overview of the NSTC and Natcast, its strategic focus areas, work to-date, and updates including R&D, workforce, facilities, and membership. Discussion of opportunities for collaboration between Microelectronics Commons and the NSTC.

R&D and Workforce Development
Join Natcast and semiconductor ecosystem leaders in panel and discussion sessions focused on research and development topics and workforce development initiatives.

Shark Tank-Style Event
Emerging innovators will pitch their ideas in this fun and interactive session.

Thank you

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membership@natcast.org

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